User's Manual

R-Car M2 Application Development Board Hardware Manual

R-S Part Number

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Revision History	R-CarM2 Application Development Board Hardware Manual

Revision	Date	Description	
		Page	Modification
1.00	Feb. 24, 2015	-	First revision issued.

Contents

Tables

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1. Overview

The R-CarM2 is a new generation SOC featuring the midrange functionality required for the next generation of car infotainment systems. Its newly employed bus configuration maximizes system performance, space saving, and cost efficiency.

The R-CarM2 Application Development Board, is an R-CarM2-specific evaluation board that can be used to evaluate solutions using the R-CarM2 and to develop operating systems, device drivers, and applications. Using the R-Car M2 Application Development Board allows the developers to efficiently conduct required tasks such as evaluation of the R-CarM2 system performance and thus greatly reduces the turn-around time in product development.

1.1. Features

1.1.1. The R-CarM2 includes:

- Two 1.0-GHz ARM Cortex™-A15 MPCore™ cores (dual core: option)
- Realtime processing core SH-4A: 780MHz (option)
- Memory controller for DDR3-SDRAM (DDR3-1333) with 32 bits × 1 channel
- Three-dimensional graphics engines
- Video processing unit
- Sound processing unit
- SD card host interface (3 channels), MMCIF (1 channel)
- USB2.0 host (1 channel), USB2.0 host/function (1 channel)
- DU (digtal RGB 2 channels), DCU, TCON, VIN (2 channels), IMR-LX2
- VSP1, VCP3, FDP1, 2D-DMAC
- ADSP (option), SCU, SSIU (10 channels), MediaLB+, MLM, DTCP, ADG
- Crypto engine (option)
- CAN, IE-BUS, Ethernet MAC, Ethernet AVB
- WDT, TPU, CMT1, TMU, CPG, INTC, DMAC, LBSC
- I^2C (5 channels), IIC (2 channels), SCIF (6 channels), SCIFA (6 channels), SCIFB (3 channels), MSIOF (3 channels), QSPI, HSCIF (3 channels), PWM (7 channels)
- GPIO, etc
- Power supply voltages (typ.) 3.3 V, 1.8 V, 1.5 V/1.35 V, 1.0 V

1.1.2. The R-Car M2 Application Development Board includes:

Table 1.1.1 List of R-Car M2 Application Development Board Functions (1)

The PORTER board Function List. Page 1 of 2			
Board Function	Module	Description	Note
RAM	DDR3	Dual Channel DDR3-1600, 1GByte x2 channels, 32bit data width x2 channels	Micron MT41K256M16HA-125 x4
		4G bit(16bit data width) x4 devices.	
		SDRAM Backup feature: Not Supported	
	LBSC	No device	
ROM	LBSC	NOR Flash on board:	Pin Multi: QSPI
		128MB NOR Flash: Spansion S29GL01GP11TFIR10	Related Jumper: JP2, SW18
		Databus width 16 bit	
		64MB x2banks or 128MB x1bank	
	QSPI	SPI Flashon board:	Pin Multi:
		Spansion S25FL512SAGM FIG11 (512M bit=64MB) x1 device.	LBSC_A[25:20]
Debug I/F	DBG	Connector. HTST-110-01-S-DV (20pin)	
	DBG2	---	not supported
	GPIO	LED x3 devices 'GPLED' for General Purpose. (LED2~LED4)	GPIOs: GP2_19, GP2_20. GP2_21
	SCIF0	Debug Serial x 1 (TX, RX)	
		USB to UART Bridge	
		SILICON LABS CP2102-GM x1 (Bridge spec: max 1Mbps)	
		Connector. USB Type miniAB	
	SCIF1	---	not supported
LAN	EtherMAC	Debug Ether(100Mbps)	For Interrupt:
		RMII PHY:	IRQ0
		MICREL KSZ8041RNLI	For Reset:
		Connector:	GP5_22 (AVB_TXD4)
		CN10: TDK TLA-6T776F	Pin Multi:
		EXIO Connector B (CN3: QSH-030-01-L-D-A-K)	EtherAVB
SATA I/F	SATA0	3Gbps, Gen2	Pin Multi:
		Connector 67491-0020	USB3.0
PCIE I/F	PCI express	PCI Express Base Specification Revision 2.0, 1-lane, 2.5GT/s or 5.0GT/s	Pin Multi:
		Connector. 87715-9006	SATA1
USB 2.0 I/F	USB2.0 ch0	USB2.0 Host or Function	
		Connector Type miniAB.	
	USB2.0 ch1	USB2.0 Host	
		Connector Type A	
MLB+ I/F	MLB+ (MOST)	6wire-MOST Interface(150Mbps)	
		Connector: CN23 : QSE-060-01-F-D-A	
SDHI	SDHI0	Connector:	For voltage control:
		SD Card slot.	GP2_12
		Interface voltage:	
		Either 3.3V or 1.8V.	
	SDHI1	---	not supported
	SDHI2	Connector:	For voltage control:
		microSD Card slot, DBG3 can be connected instead of microSD card.	GP2_26
		Interface voltage:	Pin Multi:
		Either a 3.3V or 1.8V	MMC
MSIOF	MSIOF0	Renesas Electronics R2A11302FT	
		Connector:	
		EXIO Connector (CN6: 3M 961106)	
Video Output	DU0_LVDS	LVDS output.	
		5 pair (CLK, CH0~CH3)	
		Connector:	
		Signal: CN30: Hirose DF14A-20P-1.25H(55), TouchScreen: CN31: JST GB10B-XH-AMLFSNP	
	DU1	HDMI output	
		HDMI Transmitter.ADV7511WBSWZ	For Interrupt:
		Connector: Type A Receptacle	GP3_29 (DU1_ODDF_3)
		CN45: Tyco 1747981-1	
Video Input	VIN0	YCbCr 8bit. BT656	
		Video Decoder. Analog Devices ADV7180WBCP32Z, Connector: CN15: RCA Composite Video	
	VIN1	Connector:	Pin Multi:
		EXIO Connector B (CN3 : QSH-030-01-L-D-A-K)	EtherAVB

Table 1.1.2 List of R-Car M2 Application Development Board Functions (2)

The PORTER board Function List. Page 2 of 2			
Board Function	Module	Description	Note
Audio	SSI0, SSI1,	Either [A] or [B]	
	SSI2, SSI9	[A] Audio Output(SSI0), Input(SSI1)	Note:
		Codec: AKM AK4642EN x1	SSI channles connected to AK4642
		Connector: mini jack x1 for stereo line output	can be selected by JP3 (AK4642 default)
		Connector: mini jack x1 for stereo line/MIC input	
		[B]Audio Multi-Channel Output.(SSI0, SSI1, SSI2, SSI9)	Related Jumper: JP3
		HDMI Transmitter ADV7511WBSWZ	
		Connector: HDMI standard type A	
	SSI3, SSI4	EXIO Connector A (CN23 : QSE-060-01-F-D-A)	Note:
			Connect to CN23 as GPIO2_9,10,11,14
	SSI5, SSI6	EXIO Connector A (CN23 : QSE-060-01-F-D-A)	Note:
			Connect to CN23 as GPIO2_15,16,17,18
CAN	RCAN	CN11 : B3B-XH-A	
		This interface is connected to the following devices.	Related Jumper: JP4
		CAN tranceiver Renesas HA13721FPK (5V)	
IEBUS	IEBUS	CN12 : B4B-XH-A	
		This interface is connected to the following devices.	
		IEBUS tranceiver Renesas HA12240FP	
I2C I/F	I2C1	Interface voltage: 3.3V	
		This interface is connected to the following device:	
		PMIC DA9063 (Alternative/HS-I2C)	
	I2C2	Interface voltage: 3.3V	
		This interface is connected to the following devices:	
		HDMI Transmitter ADV7511, Video decoder ADV7180,	
		Audio Codec AK4642, I2C EEPROM	
	I2C4	Interface voltage: 3.3V	Note:
		This interface is connected to the following device:	for LCD touch panel control
		Pin header (CN31 : JST (G)B10B-XH-AM(LF)(SN)(P))	
	I2C5	Interface voltage: 1.8V	
		EXIO Connector A (CN23 : QSE-060-01-F-D-A)	
	I2C6	Interface voltage: 1.8V	
		This interface is connected to the following devices:	
		PMIC DA9063, and DA9210 (PM-I2C)	
EXIO	various	EXIO Connector A CN23	
Connector	modules	samtec 120pin.QSE-060-01-F-D-A	
		EXIO Connector B CN3	
		samtec 60pin.QSH-030-01-L-D-A-K	
Power IC		International Rectifier: IR3838MPbF (12V->5V)	
		Dialog Semiconductor: DA9210, DA9063 (5V-> 3.3V, 1.8V)	
		Richtek: RT7239GSP (12V -> 1.35V)	
		Richtek: RT9026GSP (1.35V -> Vtt)	
		Diodes Incorporated: ZLDO1117G-25 (3.3V->2.5V)	
		Diodes Incorporated: ZLDO1117G-12 (3.3V->1.2V)	
Power Supply	—	DC12.0V input	
Board size	—	170mm x 125mm	

1.2. Usage Notes

1.2.1. R-Car M2 Application Development Board Specifications

- **Take particular care to ensure the correct configurations of the jumpers and switches mounted on the R-Car M2 Application Development Board. Incorrect configurations may damage on-board devices.**

- **For the R-Car M2 Application Development Board, be sure to use the power supply that comes with it. Applying a voltage greater than 12 V may damage devices on the R-Car M2 Application Development Board.**

- **There are sequences for turning on and off the power supply to the R-CarM2. For the R-Car M2 Application Development Board, be sure to obey the notes below.**

  (1) When power is turned on

  Be sure to confirm that the ACC switch (SW26) is off before plugging the AC adapter into the power source.

  It is prohibited to plug the AC adapter into a power source while the ACC switch (SW26) is on.

  (2) When power is shut off

  Be sure to turn off the ACC switch (SW26) before unplugging the AC adapter from the power source.

  It is prohibited to unplug the AC adapter from the power source while the ACC switch (SW26) is on.

- **The maximum current draw for the VSYS and D5.0V pins on the R-Car M2 Application Development Board is 7A each. Therefore, operation should be such that the current drawn by either pin does not exceed 7A. Also ensure that the current draw does not exceed 7A if an IO expansion board or external storage device is connected to the R-Car M2 Application Development Board.**

1.3. Board Configuration

The R-Car M2 Application Development Board is composed of a single board whose size is 170 mm × 125 mm.
Figure 1.3.1 shows a block diagram of the R-Car M2 Application Development Board.
Figure 1.3.2 is a memory map of the R-Car M2 Application Development Board.

1.3.1. Block Diagram of R-Car M2 Application Development Board

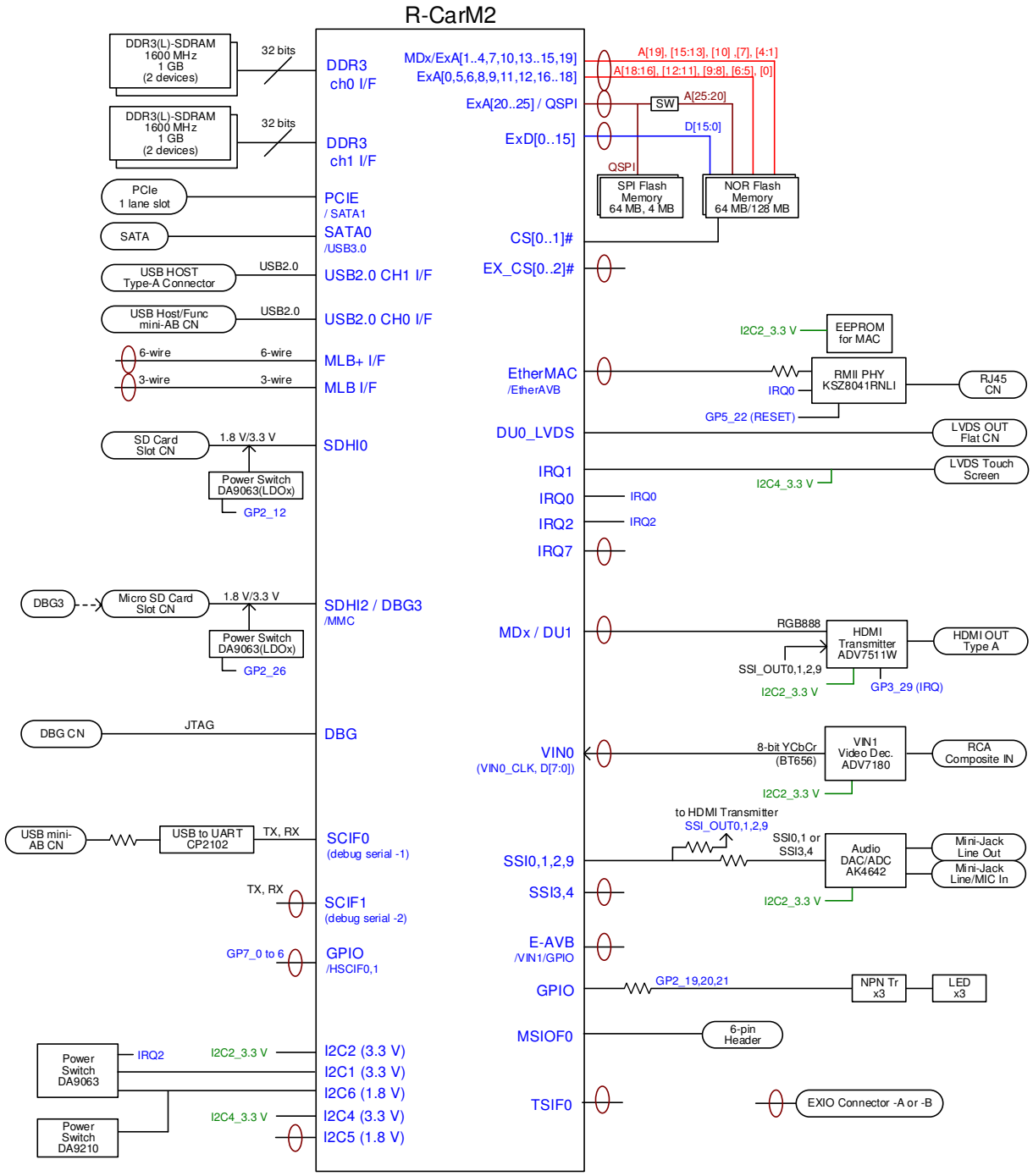


Figure 1.3.1 **Block Diagram of R-Car M2 Application Development Board**

1.3.2. Address Map of R-Car M2 Application Development Board

The address map of the LBSC space is shown below.
For the DDR3L memory space, see the section DDR3L-SDRAM Interface.
For other address space, see the Hardware section in the R-Car Series, 2nd Generation User's Manual

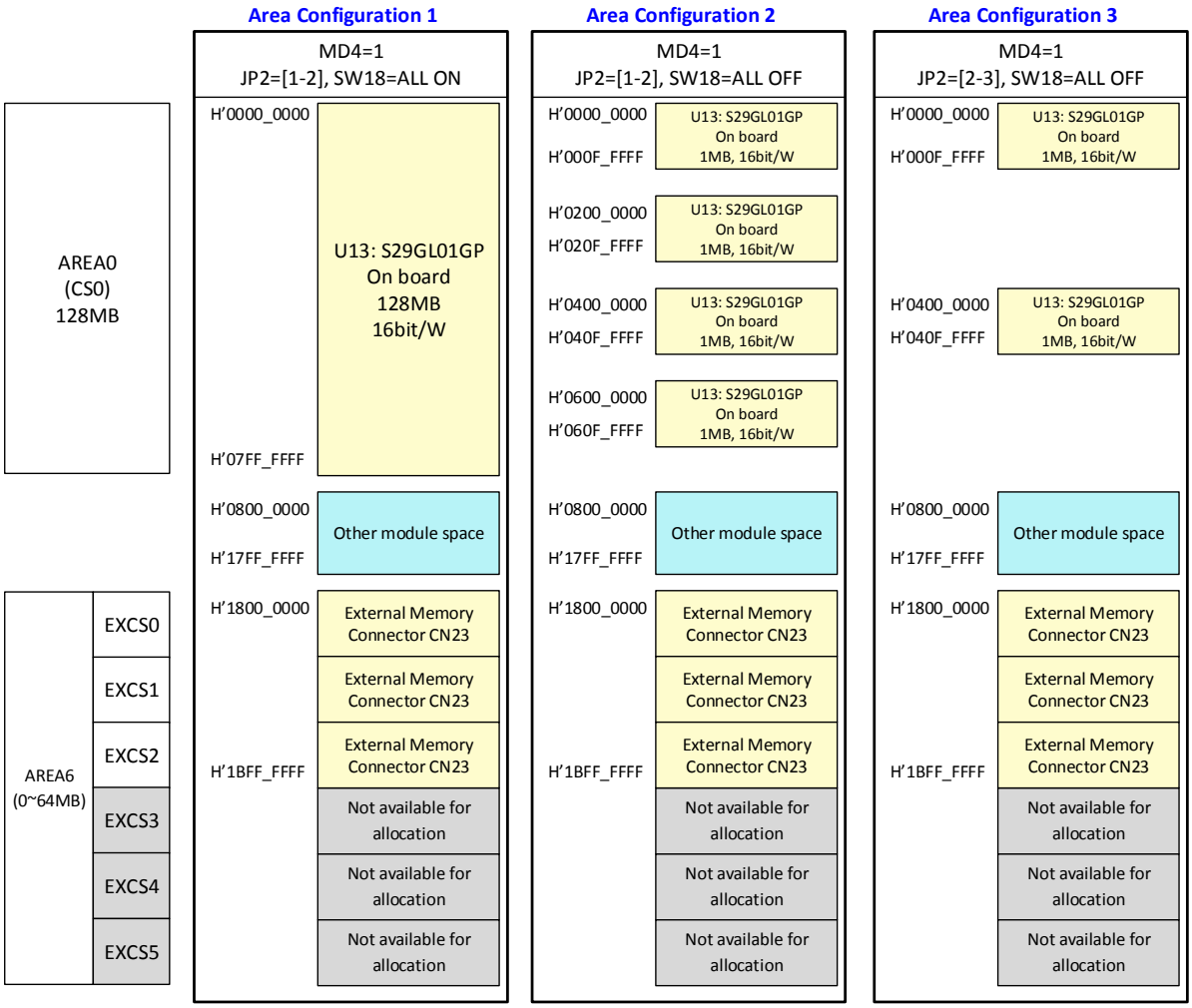


Figure 1.3.2 **Address Map of R-Car M2 Application Development Board**

2. R-Car M2 Application Development Board Interface Module Specifications

2.1. Mode Setting

2.1.1. Specifications

The operating mode of the R-CarM2 is set by a power-on reset. Each of the mode pins is set by pull up or pull down resistors, mounted on the development board. Several may also be changed by jumpers. For details on each operating mode, see the documents related to the R-CarM2 operating mode specifications.

2.1.1.1. MD0 Pin — Selection of Free-Running Mode or Step-Up Mode

This pin selects the free-running mode or step-up mode.

MD0	Free-Running Mode or Step-Up Mode
0	Free-running mode
1	Step-up mode

2.1.1.2. MD[3:1] Pins — Selection of Boot Device

These pins select the boot device.

MD3	MD2	MD1	Selection of Boot Device
0	0	0	Boot from area 0 (boot from the external mask ROM)
0	1	0	QSPI (48.75 MHz/16-Kbyte transfer)
0	0	1	Reserved
0	1	1	Reserved
1	0	0	QSPI (39 MHz/16-Kbyte transfer)
1	0	1	Reserved
1	1	0	QSPI (39 MHz/4-Kbyte transfer)
1	1	1	Reserved

2.1.1.3. MD4 Pin — Selection of CS0 Space Size

This pin selects whether the area 0 space (CS0) is used as a normal space (64 Mbytes) or an expanded space (128 Mbytes).

MD4	Area Division
0	Area 0: 64 Mbytes
1	Area 0: 128 Mbytes

2.1.1.4. MD5 Pin — Selection of Secure or Non-Secure Mode

This pin selects the secure or non-secure mode

MD5	Selection of Secure or Non-Secure Mode
0	Secure (When LCS = Secure, the value read from the register for MD5 is forcibly set to 0.)
1	Non-secure

2.1.1.5. MD[7:6] Pins — Selection of Master Boot Processor

These pins select the master boot processor.

MD7	MD6	Selection of Master Boot Processor
0	0	CA15 boot
0	1	Reserved
1	0	SH boot (32 bits)
1	1	Reserved

2.1.1.6. MD8 Pin — Selection of Area 0 Space Data Bus Width

This pin sets the data bus width of the area 0 space (CS0) to 8 bits or 16 bits. Select the data bus width of the boot device connected to the LBSC.

MD8	EXBUS Area 0 Data Bus Width
0	8-bit bus
1	16-bit bus

2.1.1.7. MD9 Pin — Selection of Crystal Resonator or Crystal Oscillator

This pin selects either a crystal resonator or a crystal oscillator to be connected to the EXTAL/XTAL pins. A crystal oscillator (X6: 20 MHz) is mounted on the R-Car M2 Application Development Board by default. The crystal resonator (X5) and its peripheral circuit are not mounted.

MD9	EXTAL/XTAL Pin Setting
0	An external clock is input to the EXTAL pin.
1	A crystal resonator is connected to the EXTAL and XTAL pins.

2.1.1.8. MD12 — Reserved

Do not change the initial setting at shipment (MD12 = 0).

2.1.1.9. MD21, MD20, MD11, MD10, and MDT[1:0] Pins — Switching of JTAG, SDHI1, and SDHI2

These pins select the debugging function through the JTAG connector (CN1) or the SD card slot. Debugging through SDHI1 or SDHI2 is possible by the combination of MD pin settings in the R-CarM2 specifications, but not available on the R-Car M2 Application Development Board.

MD10	MD[21:20]	MD11	MDT[1:0]	JTAG	SDHI1	SDHI2
0	00	-	--	Boundary scan	Normal function	Normal function
0	10	0	--	Coresight (*1)	Normal function	Normal function
0	10	1	00	Coresight (*1)	Tensilica	Normal function
0	10	1	01	Coresight (*1)	SH-X4	Normal function
0	10	1	10	Coresight (*1)	Normal function	Tensilica
0	10	1	11	Coresight (*1)	Normal function	SH-X4
0	11	0	--	SH-X4	Normal function	Normal function
0	11	1	00	SH-X4	Coresight (*1)	Normal function
1	01	0	--	Coresight (*1)	Normal function	Normal function
1	01	1	00	Coresight (*1)	GPS	Normal function
1	01	1	01	Coresight (*1)	SH-X4	Normal function
1	10	0	--	SH-X4	Normal function	Normal function

(*1) “Coresight” is an abbreviation of “Coresight debug port”.

2.1.1.10. MD[14:13] Pins — Frequency Mode Setting

These pins select the frequency mode. A crystal oscillator (X6: 20 MHz) is mounted on the R-Car M2 Application Development Board. Do not change the initial setting at shipment (MD14 = 0, MD13 = 1).

MD14	MD13	EXTAL Frequency	EXTAL Divider	PLL1 (CPGM Main)	PLL0 (CPGMC)	PLL3 DDR1600/DDR1333 MD19 = 0/MD19 = 1
0	0	15 MHz	× 1/1	×208 VCO = 3120 MHz	×172 VCO = 1290 MHz	×106/×88 VCO = 1590 MHz/1320 MHz
0	1	20 MHz	× 1/1	×156 VCO = 3120 MHz	×130 VCO = 1300 MHz	×80/×66 VCO = 1600 MHz/1320 MHz
1	0	26 MHz	× 1/2	×240 VCO = 3120 MHz	×200 VCO = 1300 MHz	×122/×102 VCO = 1586 MHz/1326 MHz
1	1	30 MHz	× 1/2	×208 VCO = 3120 MHz	×172 VCO = 1290 MHz	×106/×88 VCO = 1590 MHz/1320 MHz

2.1.1.11. MD19 Pin — Selection of DDR3-SDRAM Bus Clock

This pin selects the frequency of the DDR3-SDRAM bus clock.

MD19	Switching of DDR Clock
0	DDR3-1600 mode
1	DDR3-1333 mode

2.1.1.12. MD28, MD27, and MD22 Pins — Selection of DDR Mode and MTSB Mode

These pins select the DDR3-SDRAM interface mode and MTSB mode.

MD28	MD27	MD22	DDR 64 Bits/ 32 Bits	Remarks	
0	0	0	DDR 64 bits × 1ch	-	
		1	DDR 64 bits × 1ch	-	
	1	0	Reserved	Setting prohibited	
		1	DDR 64 bits × 1ch	User PinMAX	
1	0	0	DDR 32 bits × 1ch	-	
		1	DDR 32 bits × 1ch	-	
	1	0	DDR 32 bits × 1ch	User PinMAX	
		1	DDR 32 bits × 2ch	-	(Fixed)

Note: The MD28, MD27, and MD22 pins are fixed to "1" on the board.

2.1.1.13. MD23 Pin — Selection of SATA0 or USB3.0 Function

This pin selects the SATA0 or USB3.0 function. MD23 is fixed to "0" on the R-Car M2 Application Development Board.

MD23	Selection of SATA0 or USB3.0
0	SATA0 (fixed)
1	USB3.0

2.1.1.14. MD24 Pin — Selection of SATA1 or PCIE Function

This pin selects the SATA1 or PCIE function. MD24 is fixed to "1" on the R-Car M2 Application Development Board.

MD24	Selection of SATA1 or PCIE
0	SATA1
1	PCIE (fixed)

2.1.2. Initial Values of Mode Setting Pins on R-Car M2 Application Development Board

Table 2.1.1 **Initial Values of R-CarM2 Mode Setting Pins on R-Car M2 Application Development Board**

MD Pins	Initial Value	Initial Function
MD0	0	Free-running mode
MD[3:1]	010	Boot from QSPI
MD4	0	CS0 space size (64 Mbytes)
MD5	1	Non-secure mode
MD[7:6]	00	Cortex-A15 boot
MD8	1	CS0 space data bus width (16 bits)
MD9	0	Crystal oscillator is used.
MD12	0	-
MD10, MD[21:20], MD11, MDT[1:0]	0,00,0,00	JTAG (CN1) = Boundary SCAN SDHI1 and SDHI2 = Normal function
MD[14:13]	01	Input frequency = 20 MHz
MD19	0	DDR3-1600 mode
MD28, MD27, MD22	111	DDR 32 bits × 2ch
MD23	0	SATA0
MD24	1	PCIE

2.1.3. Multiplexing and Method of Setting for Mode Setting Pins

The following table covers the pin functions that are multiplexed with the mode pins of the R-CarM2, and how the individual mode pins are set. For the mode pins that are used with fixed values, resistors are used to set them to their fixed values according to the initial settings in table 2.1.1, Initial Values of R-CarM2 Mode Setting Pins on R-Car M2 Application Development Board. Such mode pins are described as "Fixed by a resistor" in the Setting Method column in the table below.

Table 2.1.2 **Pin Multiplexing of Mode Setting Pins of R-CarM2**

MD Pin	Pin Function	Strapping Options	Setting Method	Default
MD0	DU1_CDE (GPIO)	Free-running (0)/Step-up (1)	Fixed by resistor	PULLED-UP(1)
MD1	DU1_DISP	Selects boot device	Fixed by resistor	PULLED-UP(1)
MD2	DU1_VSYNC		Fixed by resistor	PULLED-UP(1)
MD3	DU1_HSYNC		Fixed by resistor	PULLED-UP(1)
MD4	WE1#	Selects area 0 size	Fixed by resistor	PULLED-UP(1)
MD5	AUDIO_CLKOUT (GPIO)	Secure (0) or non-secure (1) mode	Fixed by resistor	OFF (1)
MD6	WE0#	Selects boot processor	Fixed by resistor	PULLED-UP(1)
MD7	DACK0 (GPIO)		Fixed by resistor	PULLED-UP(1)
MD8	EX_CS5# (GPIO)	Selects EXBUS width	Fixed by a resistor	Pulled-up (1)
MD9	EX_CS3# (GPIO)	EXTAL or EXTAL/XTAL	Fixed by a resistor	Pulled-down (0)
MD10	BS#	Debugging mode	Fixed by resistor	PULLED-UP(1)
MD11	DU1_DB5		Fixed by resistor	PULLED-UP(1)
MD12	RD#	-	Fixed by resistor	PULLED-UP(1)
MD13	A3	Selects frequency mode	Fixed by a resistor	Pulled-up (1)
MD14	A19		Fixed by a resistor	Pulled-down (0)
MD15	-	-	-	-
MD16	-	-	-	-
MD17	-	-	-	-
MD18	-	-	-	-
MD19	A14	DDR clock 1600/1333	Fixed by resistor	PULLED-UP(1)
MD20	A15	Debugging mode	Fixed by resistor	PULLED-UP(1)
MD21	A13		Fixed by resistor	PULLED-UP(1)
MD22	A10	DDR, MTSB mode	Fixed by a resistor	Pulled-up (1)
MD23	A2	Selects SATA0/USB3.0	Fixed by a resistor	Pulled-down (0)
MD24	A4	Selects SATA1/PCIE	Fixed by a resistor	Pulled-up (1)
MD25	-	-	-	-
MD26	-	-	-	-
MD27	A7	DDR, MTSB mode	Fixed by a resistor	Pulled-up (1)
MD28	A1		Fixed by a resistor	Pulled-up (1)
MDT0	SIM0_CLK	Debugging mode	Fixed by resistor	PULLED-UP(1)
MDT1	SIM0_RST		Fixed by resistor	PULLED-UP(1)

2.1.4. Block Diagram of Peripheral Circuit for Mode Pins

On the R-Car M2 Application Development Board, pull-up (100 kΩ) and pull-down (10 kΩ) resistors are used to implement the settings of the mode pins that are largely used with fixed values. When changes to the settings of mode pins are likely, this can be implemented by switches which, through resistive voltage division, select the low level when turned on and the high level when turned off.
When the R-CarM2 is released from the power-on reset (when the PRESET# signal of the R-CarM2 is changed from low to high), the mode value set by the switch or resistive voltage division is input to the R-CarM2.

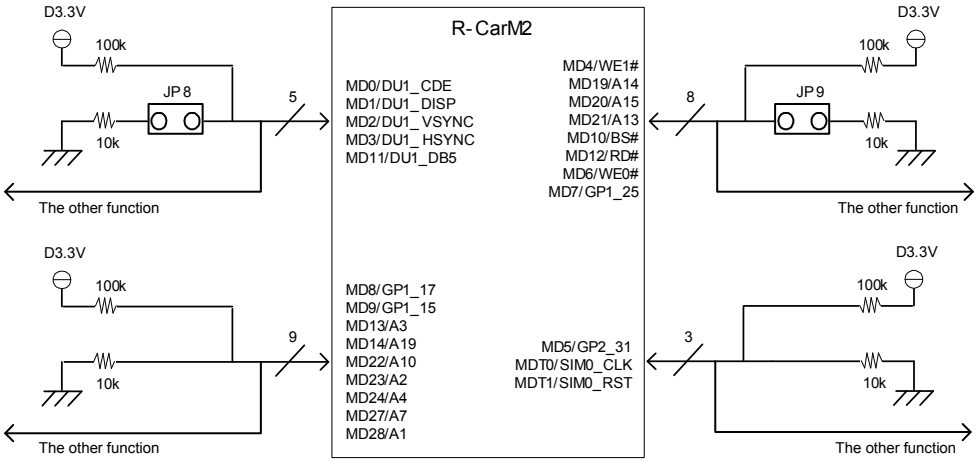


Figure 2.1.1 **Peripheral Circuit for Mode Pins on R-Car M2 Application Development Board**

2.2. DDR3L-SDRAM Interface

2.2.1. Specifications

The R-Car M2 Application Development Board incorporates four 4-Gbit DDR3-SDRAMs (16-bit bus width) (DDR: 32 bits × 2 channels) and operates at a maximum speed of DDR3-1600. On the R-Car M2 Application Development Board, the R-CarM2 and DDR3-SDRAMs are connected in 32-bit × 2-channel mode; the DDR3-SDRAMs on the channel 0 side are allocated to the address space from H'01_0000 0000 to H'01_3FFF FFFF and those on the channel 1 side are allocated to the address space from H'02_0000 0000 to H'02_3FFF FFFF. The address ranges from H'00_4000 0000 to H'00_7FFF FFFF can be accessed by default as a mirror area of H'01_0000 0000 to H'01_3FFF FFFF.

Table 2.2.1 **DDR3L-SDRAM Specifications**

Interface	DDR3L-SDRAM
Product name	MT41K256M16HA-125 AIT:E (DDR3-1600, ×16 bits, 4 Gbits) × 4 pcs
Power supply voltage	1.35 V
Capacity	Total: 2 Gbytes, Channel 0: H'01_0000 0000 to H'01_3FFF FFFF Channel 1: H'02_0000 0000 to H'02_3FFF FFFF
Bus width	32-bit data bus × 2ch
Memory bus frequency (R-CarM2 spec.)	DDR3-1600 max.

Note:
To access the address spaces for channels 0 and 1 as a single consecutive area, register settings are necessary. For details, refer to the R-CarM2 documentation.

2.2.2. Signal Correlation

Table 2.2.2 **DDR3L-SDRAM Signal Correlation**

R-CarM2 (DDR 32 bits × 2ch)	DDR3L-SDRAM			
	Channel 1		Channel 0	
	M1	M2	M3	M4
	D[31:16]	D[15:0]	D[31:16]	D[15:0]
M1DQ[31:16]	DQU[7:0], DQL[7:0]	-	-	-
M1DQ[15:0]	-	DQU[7:0], DQL[7:0]	-	-
M0DQ[31:16]	-	-	DQU[7:0], DQL[7:0]	-
M0DQ[15:0]	-	-	-	DQU[7:0], DQL[7:0]
M1A[15:0]	A[15:0]	A[15:0]	-	-
M0A[15:0]	-	-	A[15:0]	A[15:0]
M1BA[2:0]	BA[2:0]	BA[2:0]	-	-
M0BA[2:0]	-	-	BA[2:0]	BA[2:0]
M1CK1, M1CK1#	CK, CK#	-	-	-
M1CK0, M1CK0#	-	CK, CK#	-	-
M0CK1, M0CK1#	-	-	CK, CK#	-
M0CK0, M0CK0#	-	-	-	CK, CK#
M1CKE1	CKE	-	-	-
M1CKE0	-	CKE	-	-
M0CKE1	-	-	CKE	-
M0CKE0	-	-	-	CKE
M1CS1#	CS#	-	-	-
M1CS0#	-	CS#	-	-
M0CS1#	-	-	CS#	-
M0CS0#	-	-	-	CS#
M1WE#	WE#	WE#	-	-
M0WE#	-	-	WE#	WE#
M1RAS#	RAS#	RAS#	-	-
M0RAS#	-	-	RAS#	RAS#
M1CAS#	CAS#	CAS#	-	-
M0CAS#	-	-	CAS#	CAS#
M1DQS[3:2], M1DQS[3:2]#	DQSU, DQSL DQSU#, DQSL#	-	-	-
M1DQS[1:0], M1DQS[1:0]#	-	DQSU, DQSL DQSU#, DQSL#	-	-
M0DQS[3:2], M0DQS[3:2]#	-	-	DQSU, DQSL DQSU#, DQSL#	-
M0DQS[1:0] M0DQS[1:0]#	-	-	-	DQSU, DQSL DQSU#, DQSL#
M1DM[3:2]	DMU, DML	-	-	-
M1DM[1:0]	-	DMU, DML	-	-
M0DM[3:2]	-	-	DMU, DML	-
M0DM[1:0]	-	-	-	DMU, DML
M1ODT1	ODT	-	-	-
M1ODT0	-	ODT	-	-
M0ODT1	-	-	ODT	-
M0ODT0	-	-	-	ODT
M1RESET#	RESET#	RESET#	-	-
M0RESET#	-	-	RESET#	RESET#

(*) DDR_VDD/2 [V] is supplied to the M0VREFDQ[1:0] and M1VREFDQ[1:0] pins of the R-CarM2.

2.2.3. Block Diagram

The following figure shows a block diagram of the DDR3-SDRAM interface.

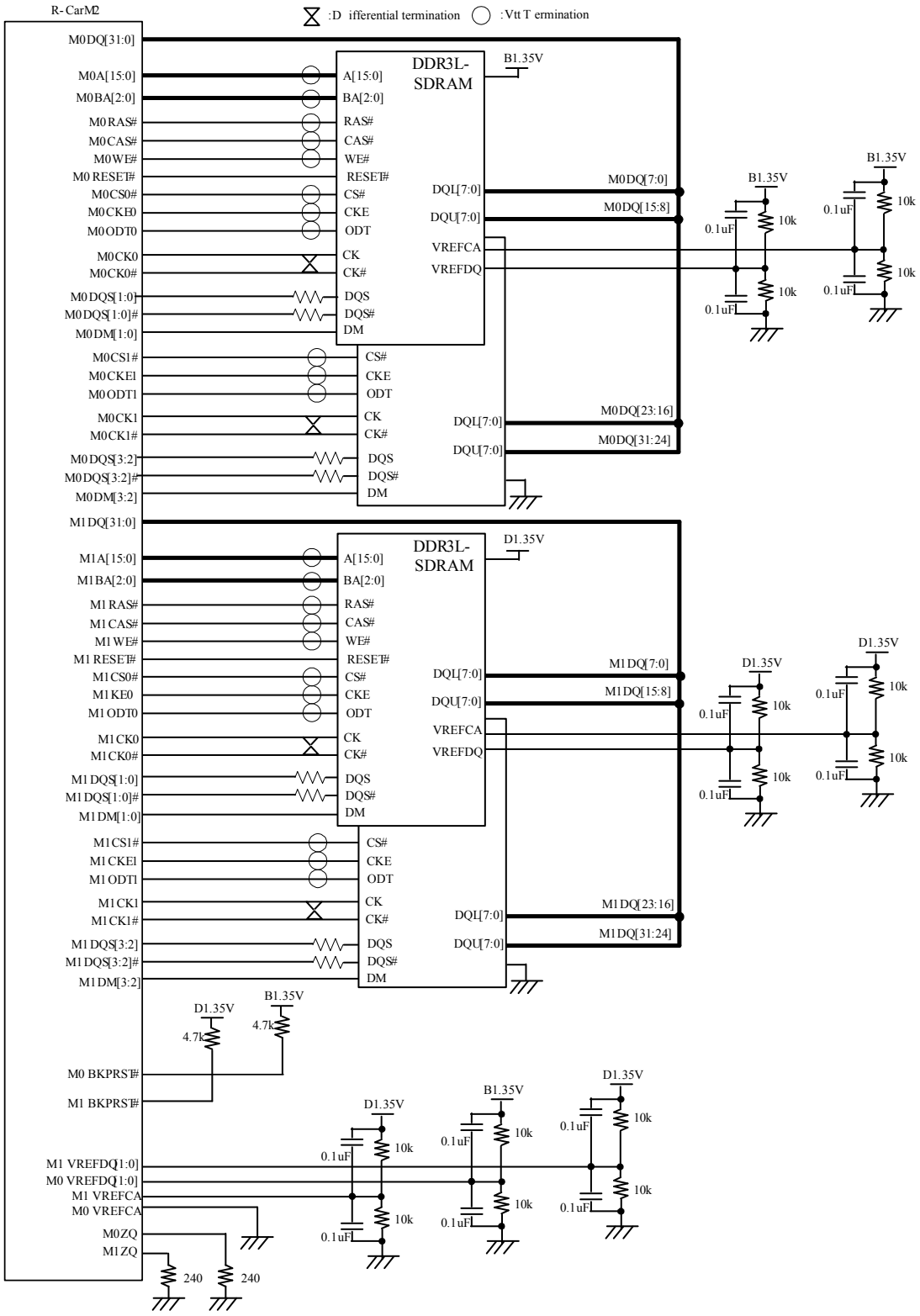


Figure 2.2.1 Block Diagram of DDR3-SDRAM Interface

2.3. Flash Memory Interface

2.3.1. Specifications

The R-Car M2 Application Development Board incorporates the S29GL01GP (1Gbit) flash memory device made by Spansion. The flash memory module can be used as 128 Mbyte space by utilizing CS1 as the most significant bit, or 64 Mbyte.

Note:
The QSPI pins are multiplexed with the higher-order address pins (A20 to A25) of the LBSC due to the specifications of the R-CarM2W's pin function controller. Accordingly, when the QSPI is in use, only the lower-order address pins (A0 to A19) of the LBSC are available for use.

Note:
When S29GL01GP is used on the R-Car M2 Application Development Board, settings of SW18 are required. Set SW18 as follows depending on the capacity.
[A] When used with the capacity of 128 Mbytes (i.e., the QSPI is not in use)
Set SW18 to all on.
[B] When used with the capacity of 1 Mbyte (A0 to A19) (i.e., the QSPI is in use)
Set SW18 to all off. 2 Mbyte capacity is possible by utilizing CS1 as the most significant address bit.

Table 2.3.1 Flash Memory Specifications

Flash memory	S29GL01GP
Operating voltage	3.3 V
Capacity	64 Mbytes or 128 Mbytes (selectable)
Bus width	16-bit data bus width

For details on the flash memory, refer to the related documents.

2.3.2. Block Diagram

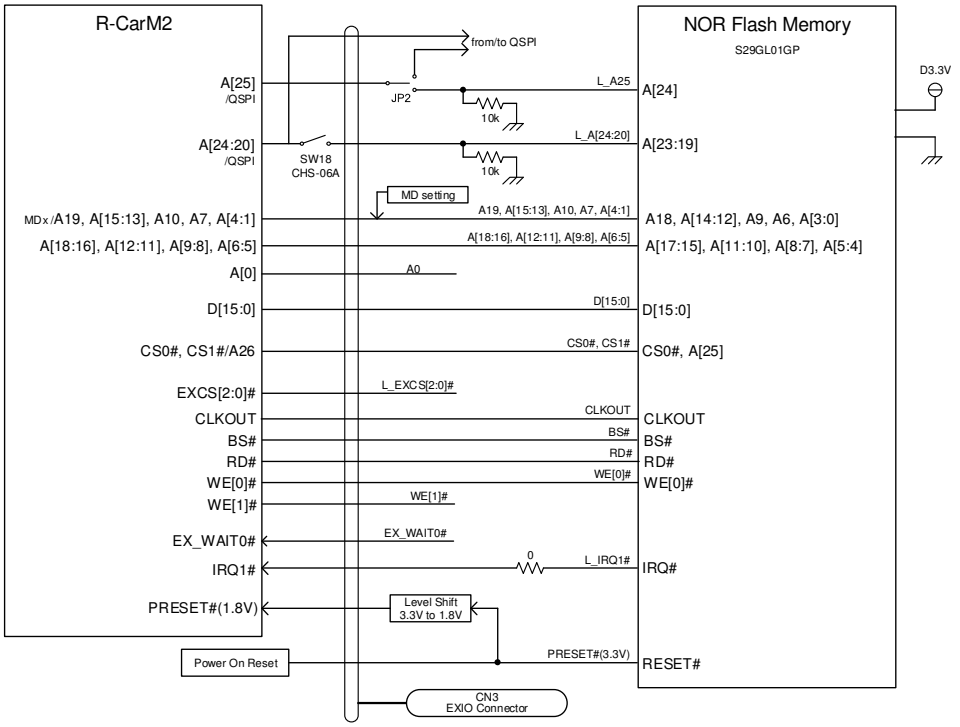


Figure 2.3.1 Block Diagram of Flash Memory Interface

2.4. SPI-Flash Interface (QSPI)

2.4.1. Specifications

The R-Car M2 Application Development Board incorporates 512-Mbit SPI flash memory devices manufactured by Spansion. The SPI flash memory devices are connected to the QSPI of the R-CarM2 via switches SW18 and jumpers JP2 and JP8. By setting SW18 and JP8, booting from the QSPI is possible. When the QSPI is to be used, set all SW18 switches to off. The QSPI pins are multiplexed with the higher-order address pins (A20 to A25) of the LBSC due to the specifications of the R-CarM2's pin function controller. Accordingly, when the QSPI is in use, only the lower-order address pins (A0 to A19) of the LBSC are available for use.

Table 2.4.1 SPI-FLASH Interface Specifications

QSPI controller	R-CarM2's on-chip QSPI module
SPI-FLASH	U: S25FL512SAGMFIG11 by Spansion (512 Mbits)
Clock rate of R-CarM2's QSPI	48.75-MHz operation (max.)

2.4.2. Block Diagram

A block diagram of the SPI flash memory interface is shown below.

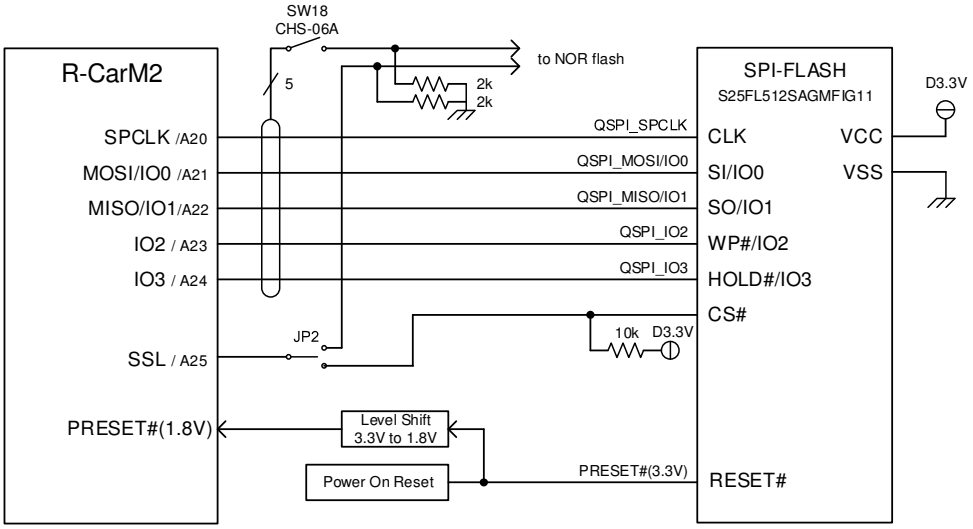


Figure 2.4.1 Block Diagram of SPI-Flash Interface

2.5. Video Input Interface

2.5.1. Specifications

The R-CarM2 has three channels of video input functions (VIN0 to VIN2). For details, see the section on video input in the R-Car Series, 2nd Generation User's Manual:Hardware.

On the R-Car M2 Application Development Board, ADV7180WBCP32Z (U22) manufactured by Analog Devices is connected to VIN0 of the R-CarM2 and used as a composite video decoder. The ADV7180WBCP32Z (U22) handles inputs in the ITU-R BT.656 8-bit (YCbCr) format according to the switch settings. The block diagram of the VIN0 interface is shown below.

The registers of ADV7180 should be set via channel 2 of the I^2C.

Table 2.5.1 Video Input Specifications

Video input module	R-CarM2's on-chip video input module channel 0
Composite video decoder for VIN1	U22: ADV7180WBCP32Z by Analog Devices I^2C-BUS ch2 slave address = H'40 for write, H'41 for read
Video input connector	CN: RCA connector for VIN1

2.5.2. Block Diagram

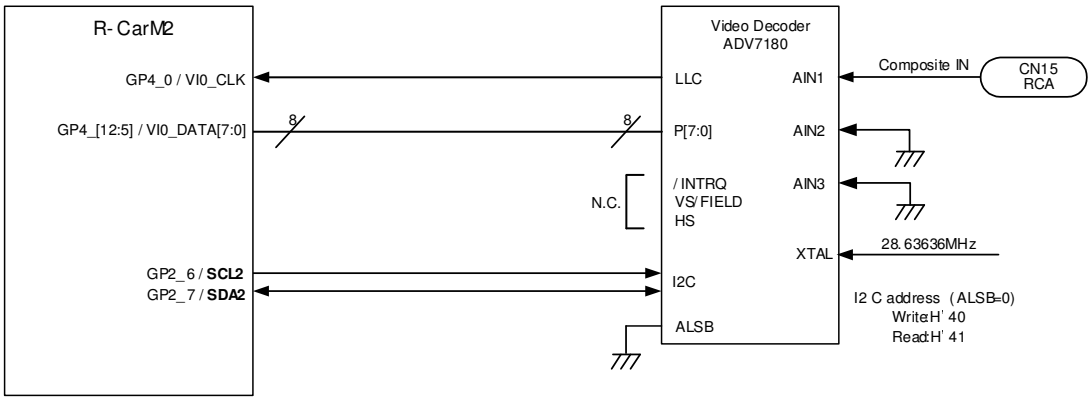


Figure 2.5.1 Block Diagram of Video Input Interface

2.6. Video Output Interface

2.6.1. Specifications

R-CarM2 incorporates one display unit (DU) with the LVDS interface and one display unit with the digital RGB interface.

On the R-Car M2 Application Development Board, the HDMI transmitter (ADV7511) converts the digital RGB signals of DU1 to HDMI signals. These digital RGB signals are also connected to the EXIO connector (CN30).

In addition, the LCD connector (CN30) is directly connected to DU_LVDS channel 0 (DU0_LVDS). T

On the R-Car M2 Application Development Board, the external dot clock inputs are connected as follows: DU0_DOTCLKIN is connected to X13 (148.50 MHz) and DU1_DOTCLKIN is connected to X2 (74.25 MHz, socket-mounted). DU1_DOTCLKIN is further connected to the EXIO connector (CN30). Alternatively, a clock signal derived by frequency-dividing the R-CarM2's internal clock can be selected. For details, see the display unit specifications in the R-Car Series, 2nd Generation User's Manual:Hardware.

Table 2.6.1 Video Output Interface Specifications

Display controller	R-CarM2's on-chip display unit
DU0_LVDS	[LVDS Output] Connector CN30: DF14A-20P-1.25H by Hirose, for LVDS signals. CN31: Backlight control and I2C / interrupt input for touch.
DU1 (digital RGB)	[HDMI Output] HDMI transmitter converts digital RGB signals to HDMI signals. U44: ADV7511WBSWZ by Analog Devices Connector CN45: 1747981-1 (HDMI type A, standard, 19-pin) by Tyco Electronics

2.6.2. Block Diagram

A block diagram of the video output interface on the R-Car M2 Application Development Board is shown below.

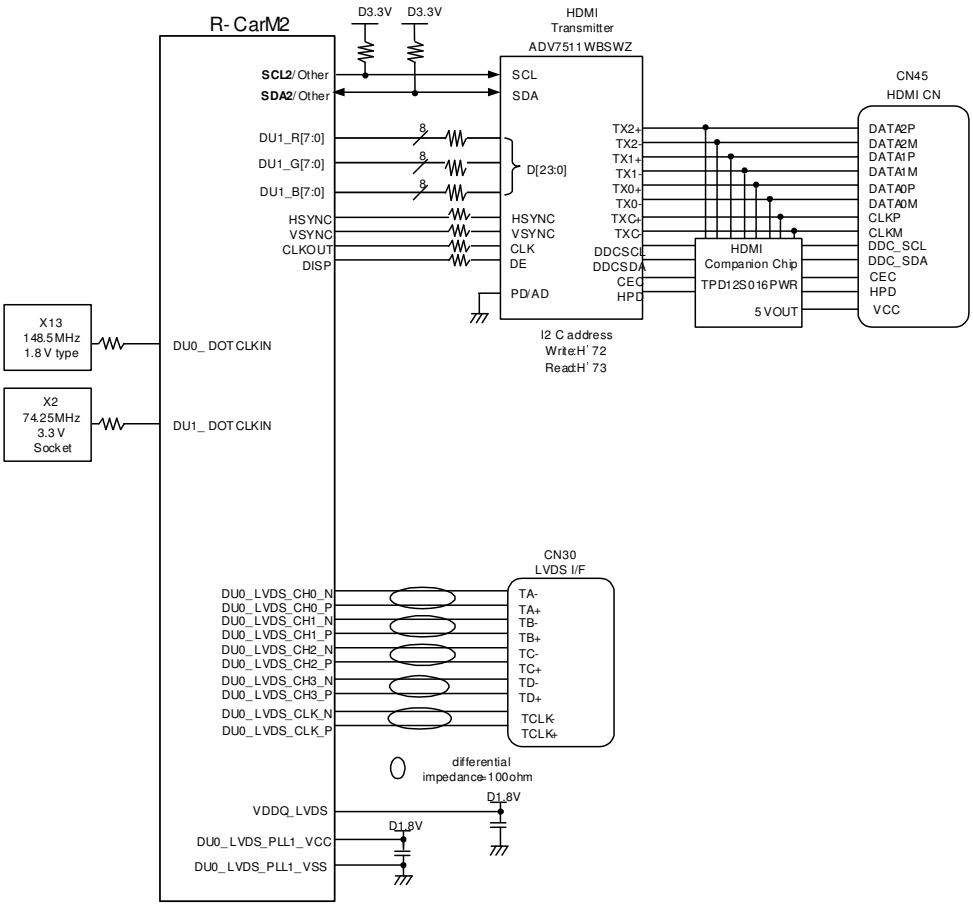


Figure 2.6.1 Block Diagram of Video Output Interface

2.7. Debugger Interface

2.7.1. Specifications

The R-Car M2 Application Development Board incorporates a debugger interface via a 20-pin connector (DBG) for connection to the JTAG emulator.

The R-CarM2 supports the DBG3 interface as a debugger interface, but the R-Car M2 Application Development Board does not include this function. The signals related to DBG3 (SDHI2) are instead connected to EXIO connector. On the R-Car M2 Application Development Board, the debugging function can be accessed through the JTAG connector CN1

Table 2.7.1 DBG Specifications

DBG interface (20-pin)	CN1: HTST-110-01-S-V by Samtec

2.7.2. Block Diagram

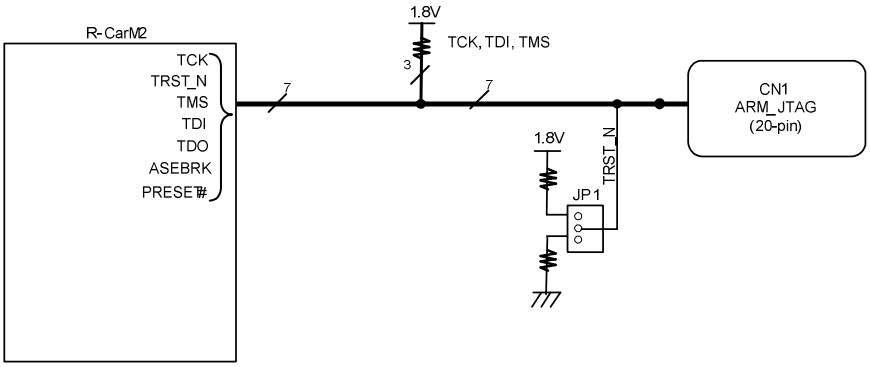


Figure 2.7.1 Block Diagram of JTAG (DBG) Interface

2.8. Debug Ether Interface (EtherMAC)

2.8.1. Specifications

The R-CarM2 incorporates the EtherMAC that supports 100Base-T or 10Base-T compliant with IEEE 802.3u. On the R-Car M2 Application Development Board, the EtherMAC signals are connected to the RMII PHY interface (KSZ8041RNLI) manufactured by Micrel. In addition, CN3 on the bottom of the board supports the REACH interface sub boards.

Table 2.8.1 Debug Ether Interface Specifications

MAC layer	R-CarM2's on-chip EtherMAC
Physical layer transceiver	U21: KSZ8041RNLI (RMII) by Micrel
Reach connector	CN3
Modular connector	CN10: TLA-6T776F (RJ-45 with pulse transformer) by TDK

2.8.2. Block Diagram

A block diagram of the debug Ether interface is shown below.

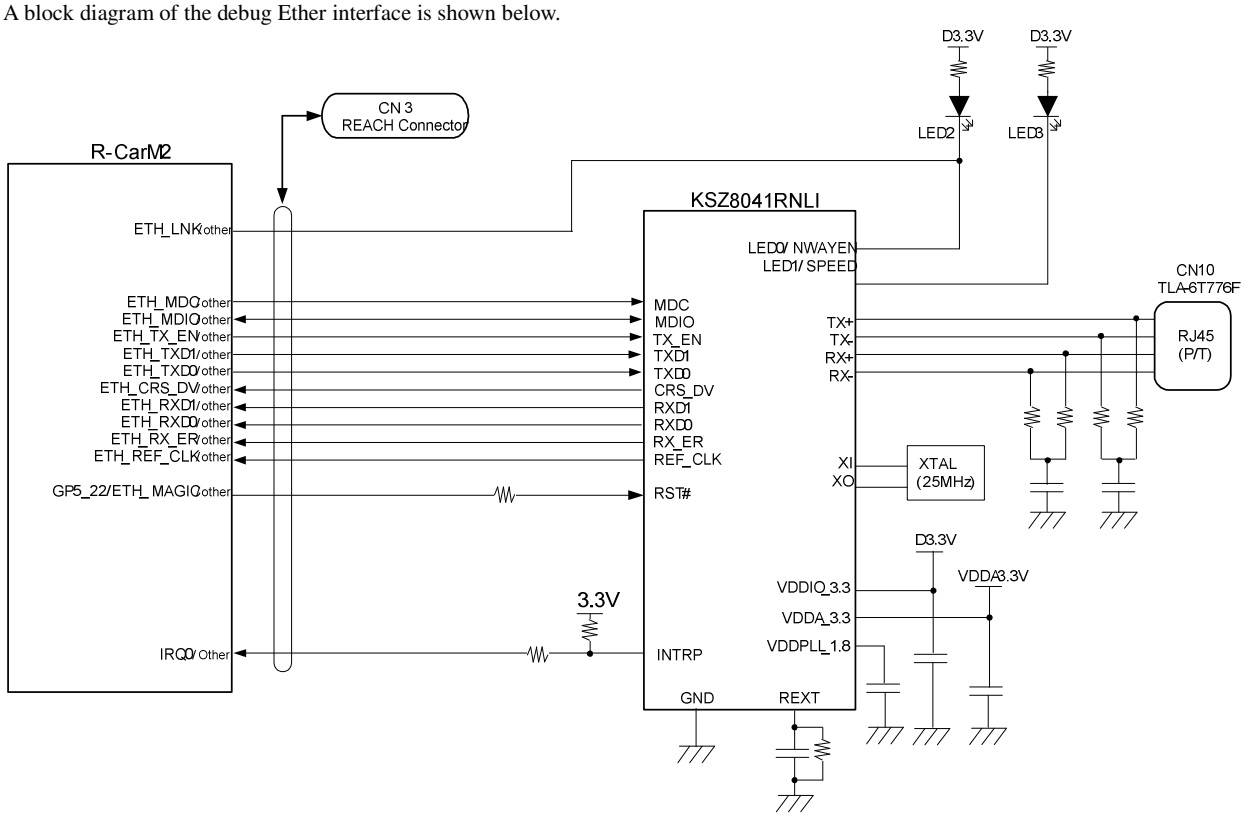


Figure 2.8.1 Block Diagram of Debug Ether Interface

2.9. Audio Codec Interface (SSI0, SSI1, SSI2, and SSI9)

2.9.1. Specifications

On the R-Car M2 Application Development Board, the codec (AK4642EN) is connected to the SSI0 and SSI1of the R-CarM2.
The PDN (power-down) pin of AK4643EN is controlled by the PRESETOUT# signal output from the R-CarM2.
The audio interface of AK4642EN is in the slave mode after PRESETOUT# is released from a reset and can be switched to the master mode by a register that is accessed via channel 2 of the I²C. Furthermore, the SSI on the R-CarM2 side can be set as the master or a slave. It is assumed that SSI_SDATA0 is set to transmit mode and SSI_SDATA1 is set to receive mode on the R-Car M2 Application Development Board.
Among the signals of the audio interface, the signals of SSI0, SSI1, SSI2, and SSI9 are also connected to HDMI transmitter ADV7511 (U44) on the R-Car M2 Application Development Board.

Table 2.9.1 SSI Codec Specifications

Controller	R-CarM2's on-chip SSI0 and SSI1
Codec	U24: AK4642EN by Asahi Kasei
Audio interface	R-CarM2 (SSI) = Master or slave selectable AK4642EN = Master or slave selectable (default: slave)
Audio connector	LINE-OUT CN13, 3.5-mm green mini-jack LINE-IN/MIC-IN CN14 3.5-mm pink mini-jack)

2.9.2. Block Diagram

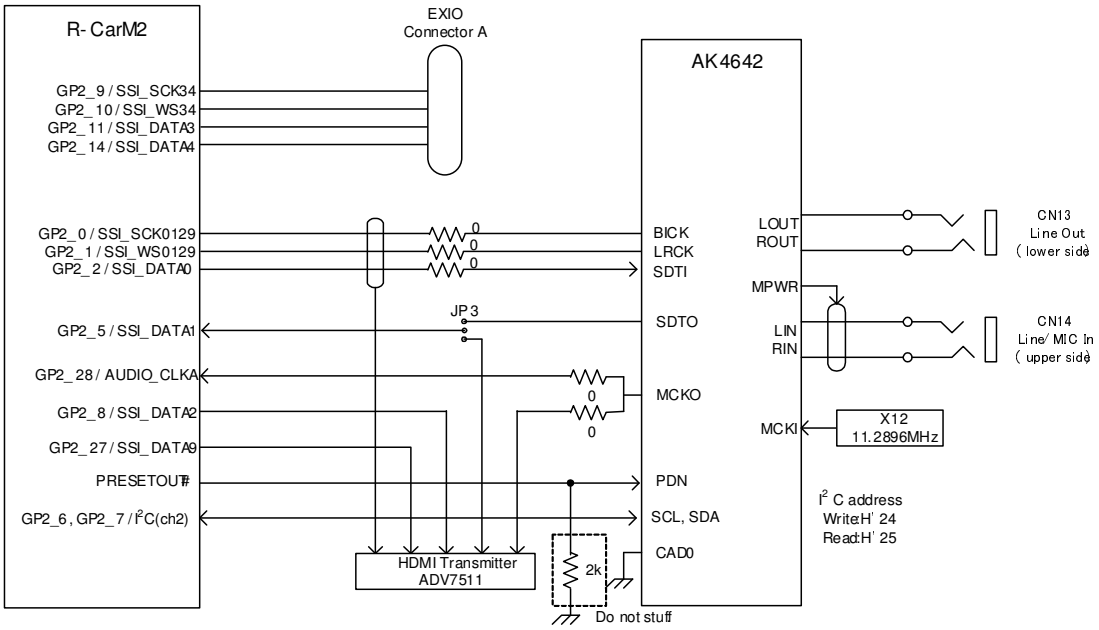


Figure 2.9.1 Block Diagram of Audio Codec Interface

PCI-Express Interface

2.9.3. Specifications

The R-Car M2 Application Development Board incorporates the PCI-Express interface for one lane (×1) as a dedicated interface for the PCI-Express bus. The on-chip PCIE module in the R-CarM2 works in either of two modes, Root Port or Endpoint, which are defined in the PCI Express specifications. In the R-CarM2, the operating mode is specified through internal register settings (mode setting register (PCIEMSR)). For details, refer to the R-Car Series, 2nd Generation User's Manual:Hardware.

Note:

To reduce the difference in wiring length between each pair of differential signals from the R-CarM2 to the PCI-Express slot, the D+ and D- line automatic swap function is used to swap the TODP1_PCIe and TODN1_PCIe signals output from the transmit pins before connection to the slot.

Table 2.9.2 PCI-Express Interface Specifications

PCI-Express controller	R-CarM2's on-chip PCI-Express controller
PCI-Express slot (1 lane)	87715-9006 by Molex (CN5)
PCI-Express clock source	IDT5V41066PGGI by IDT

2.9.4. Block Diagram

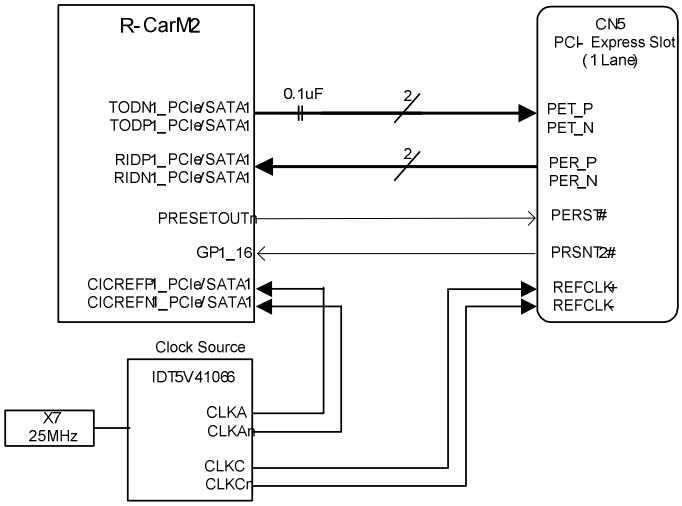


Figure 2.9.2 Block Diagram of PCI-Express Interface

2.10. Serial-ATA Interface

2.10.1. Specifications

The R-Car M2 Application Development Board incorporates one serial-ATA interface (SATA0) channel. The R-CarM2's on-chip serial-ATA interface conforms to the Serial ATA standard rev. 3.1 and supports transfer rates of 1.5 Gbps (Gen1) and 3.0 Gbps (Gen2).

The R-Car M2 Application Development Board incorporates a 4-pin power connector (CN2) for the ATAPI device. The power connector conversion cable (4-pin to 15-pin) is required to supply power to the SATA device.

Table 2.10.1 Serial-ATA Interface Specifications

Serial-ATA interface controller	R-CarM2's on-chip serial-ATA controller
Serial-ATA connector (signal)	67491-0020 by Molex (CN4)
Serial-ATA clock source	IDT5V41066PGGI by IDT

2.10.2. Block Diagram

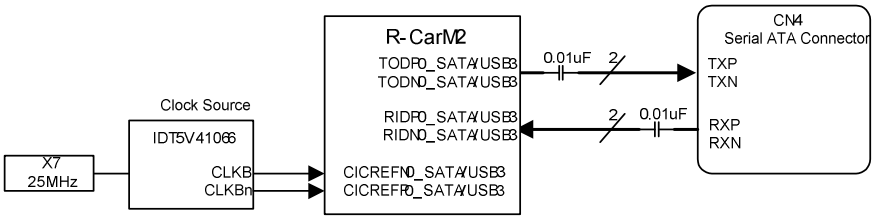


Figure 2.10.1 Block Diagram of Serial-ATA Interface

2.10.3. PCI-Express and Serial-ATA Clock Source Unit

The details on the clock source unit of the PCI-Express interface and serial-ATA interface are shown below.

IDT5V41066PGGI manufactured by IDT is used for the clock driver. This clock driver multiplies the input frequency (25 MHz) to supply a 100-MHz differential clock to the R-CarM2 and PCI-Express slot.

Note:

To reduce the difference in wiring length between each pair of differential signals from the R-CarM2 to the clock source, the P and N lines from the clock pins (CICREFP0_SATA/PCIe_18 and CICREFN0_SATA/PCIe_18 signals) are swapped before connection to the clock source.

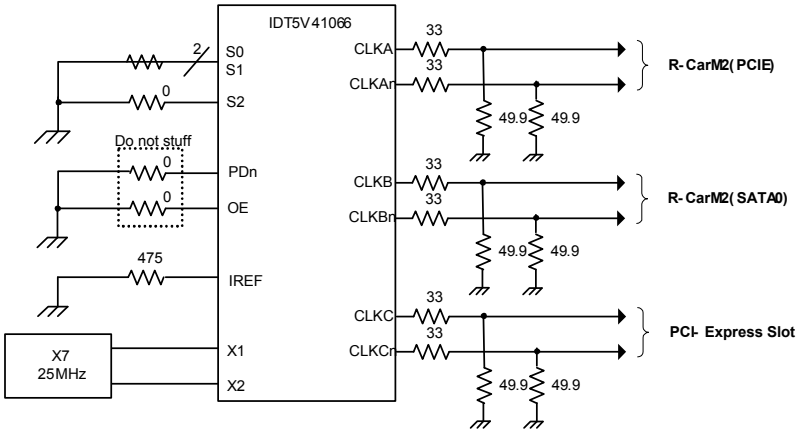


Figure 2.10.2 Block Diagram of PCI-Express and Serial-ATA Clock Source

2.11. SD Card Host Interface 0 (SDHI0)

2.11.1. Specifications

The R-Car M2 Application Development Board incorporates an SD card slot (CN8) for the on-chip SD card host interface (SDHI0) of the R-CarM2. For details on the SDHI0, see the R-Car Series, 2nd Generation User's Manual: Hardware.

On the R-Car M2 Application Development Board, the interface voltage (VCCQ_SD0) of the SD card slot can be selected by GP2_12. When GP2_12 is set to 1, 3.3 V is supplied as VCCQ_SD0. When GP2_12 is set to 0, 1.8 V is supplied as VCCQ_SD0.

Table 2.11.1 SD Card Host Interface (SDHI0) Specifications

SD card host interface	R-CarM2's on-chip SD card host interface channel 0 (SDHI0)
Interface voltage control	VCCQ_SD0 = 3.3 V (GP2_12 = '1') VCCQ_SD0 = 1.8 V (GP2_12 = '0')
SD card slot	DM1AA-SF-PEJ(82) by Hirose (CN21)

2.11.2. Block Diagram

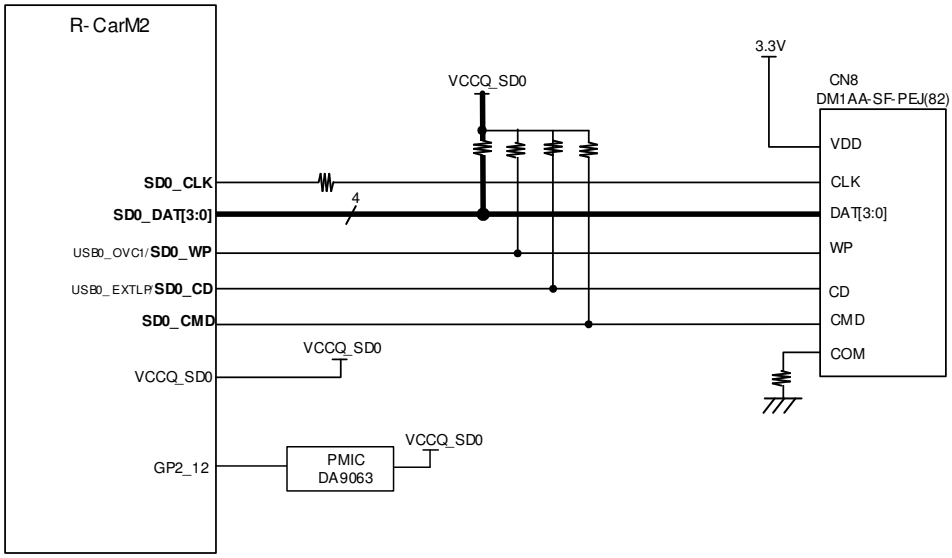


Figure 2.11.1 Block Diagram of SD Card Host Interface (SDHI0)

2.12. SD Card Host Interface 2 (SDHI2)

2.12.1. Specifications

The R-Car M2 Application Development Board incorporates a microSD card slot (CN9) for the on-chip SD card host interface (SDHI2) of the R-CarM2. For details on the SDHI2, see the R-Car Series, 2nd Generation User's Manual:Hardware.

On the R-Car M2 Application Development Board, the interface voltage (VCCQ_SD2) of the microSD card slot can be selected by GP2_26. When GP2_26 is set to 1, 3.3 V is supplied as VCCQ_SD2. When GP2_26 is set to 0, 1.8 V is supplied as VCCQ_SD2.

Table 2.12.1 SD Card Host Interface (SDHI2) Specifications

SD card host interface	R-CarM2's on-chip SD card host interface channel 2 (SDHI2)
Interface voltage control	VCCQ_SD2 = 3.3 V (GP2_26 = '1') VCCQ_SD2 = 1.8 V (GP2_26 = '0')
microSD card slot	DM3AT-SF-PEJ by Hirose (CN9)

2.12.2. Block Diagram

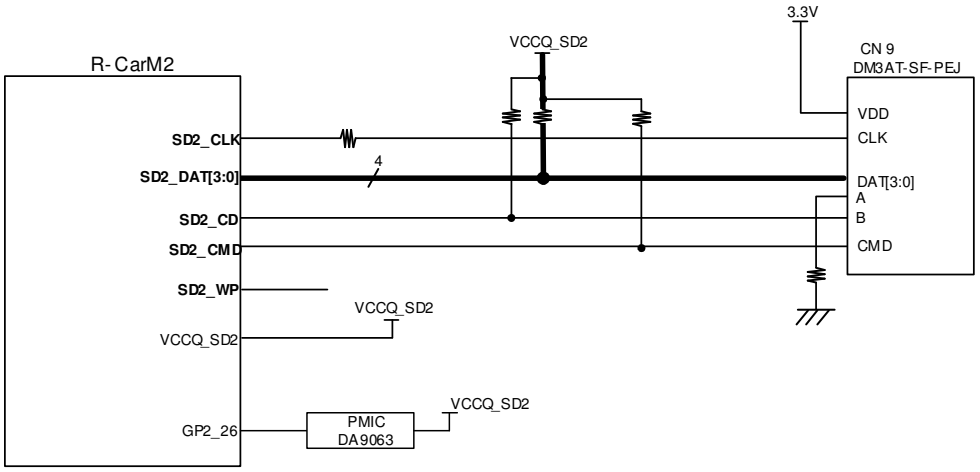


Figure 2.12.1 Block Diagram of SD Card Host Interface (SDHI2)

2.13. USB2.0 Interface

2.13.1. Specifications

The R-Car M2 Application Development Board has two USB2.0 ports that can be used as two USB2.0 host interface ports or one USB2.0 host interface port and one USB2.0 function interface port. The function interface is supported in channel 0. The MAX3355EEUD is mounted to enable use of channel 0 for evaluation of USB On-the-Go. The R-Car M2 Application Development Board incorporates a micro-AB connector as CN22 and a type A connector as CN7. For details, see the USB specifications in the R-Car Series, 2nd Generation User's Manual:Hardware and related datasheets.

Table 2.13.1 USB2.0 Specifications

USB controller	R-CarM2's on-chip USB2.0 host and function controller
USB OTG charge pump and comparators	MAX3355EEUD by Maxim Integrated Current limit: 0.2 [A] (min.)
USB power supply	BD82065FVJ by ROHM Current limit: 2.4 [A]
USB host CN	R-CarM2 USB CH1 CN7: Type A connector 67643-3911 by Molex
USB host/function CN	R-CarM2 USB CH0 CN22: mini-AB connector 56579-0576 by Molex
ESD protection diode	HZD6.2Z4 by Renesas
Common mode filter	DLP11SN900HL2 by Murata
Chip beads	BLM18PG330SN1D by Murata

* The connector for channel 0 of the USB in the R-CarM2 Application Development Board is a mini connector shared by the USB host and function.

2.13.2. Block Diagram

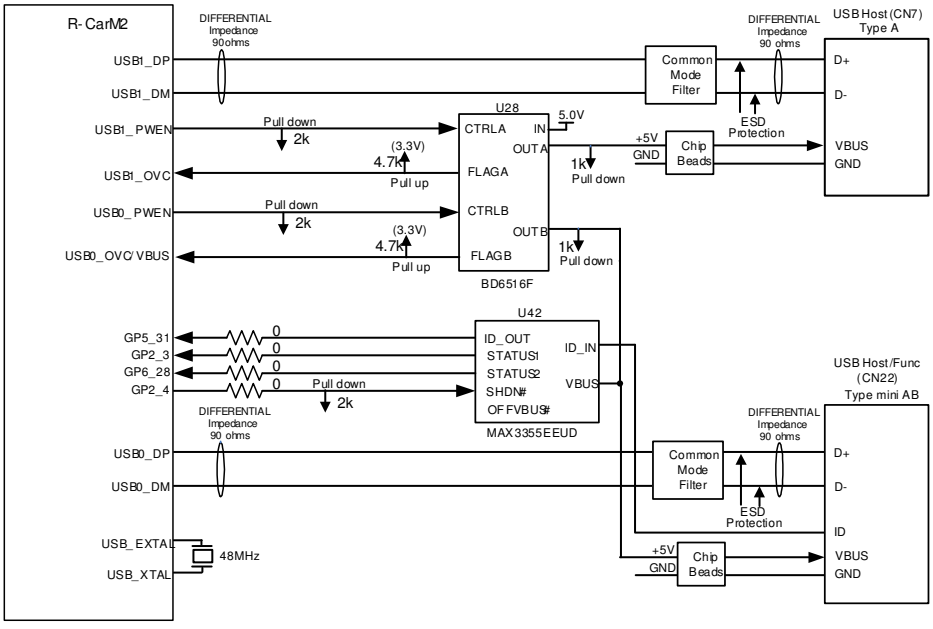


Figure 2.13.1 Block Diagram of USB2.0 Interface

2.14. Debug Serial Interfaces (SCIF0)

2.14.1. Specifications

On the R-Car M2 Application Development Board, the SCIF0 (port D) of the R-CarM2 are used as debug serial interface. The SCIF0 of the R-CarM2 is connected to the USB mini-AB connector (CN18) via the USB to UART bridge CP2102. By connecting CN18 to the host PC through a USB cable, this interface can be used as debug serial interface.

The SCIF_CLK pin of the R-CarM2 is connected to the crystal oscillator (X4) on the R-Car M2 Application Development Board, which supplies a clock frequency of 14.7456 MHz. When 14.7456 MHz is the frequency of the source clock, since the UART supports 300 bps to 1 Mbps due to the CP2102 device specifications, the maximum transfer rate becomes 921.6 kbps, which is obtained by dividing the source clock by 16. The SCIF0 has the features shown below. For details, see the SCIF specifications in the R-Car Series, 2nd Generation User's Manual: Hardware.

- Asynchronous serial communications
- Full-duplex communication supported
- Selectable bit rates by using the R-CarM2's on-chip baud-rate generator

The host PC connected to the R-Car M2 Application Development Board requires the CP2102 USB driver software. This driver software can be obtained from the following URL.

http://www.silabs.com/products/mcu/Pages/USBtoUARTBridgeVCPDrivers.aspx

Table 2.14.1 Debug Serial Interface Specifications

Serial controller	R-CarM2's on-chip SCIF0 (port D)
USB to UART bridge	CP2102 (1 Mbps max.) by Silicon Laboratories
Connector	CN18: SCIF0, ZX62D-AB-5P8 by Hirose

2.15. Reset

2.15.1. Specifications

In the R-Car M2 Application Development Board specifications, the power-on reset signal is cleared by the reset IC MAX708SCSA, 200 ms after the 3.3-V power supply has settled. The power supplies for other voltage levels, 12.0 V, 5.0 V, 1.8 V, 1.5 V, and 1.0 V, are not monitored.

A power-on reset signal can be generated by pushing the push switch (SW9). The reset signal is level-shifted from 3.3 V to 1.8 V by the HD74ALVC1G07 and is input to the PRESET# pin of the R-CarM2.

Table 2.15.1 RESET Specifications

Reset IC	MAX708SCSA by Maxim Integrated • Threshold voltage: 2.93 V • Reset delay time: 200 ms

2.15.2. Block Diagram

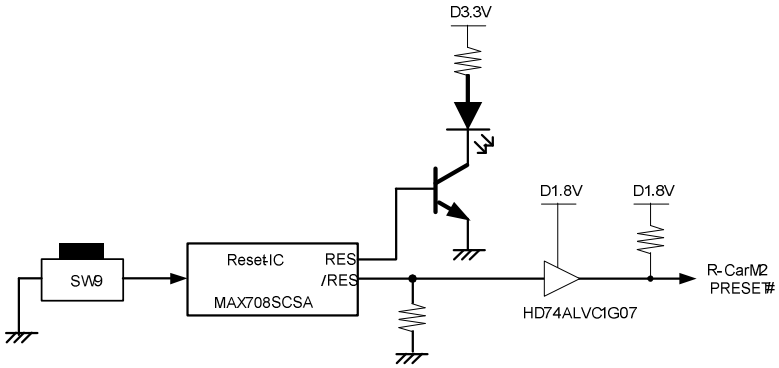


Figure 2.15.1 Block Diagram of Reset Circuit

2.16. I²C Interface

2.16.1. Specifications

The R-CarM2 incorporates seven I²C interface channels. Channels 5 and 6 are 1.8-V interfaces and channels 0 to 4 are 3.3-V interfaces. The following devices are connected to each channel of the I²C interfaces on the R-Car M2 Application Development Board.

Table 2.16.1 I2C Interface Specifications

I²C controller	R-CarM2's on-chip I²C controller
I²C devices through I²C (ch5)	[1.8 V] CN23: External IO Connector
I²C devices through I²C (ch6)	[1.8 V] U37: DA9063 by Dialog Semiconductor U38: DA9210 by Dialog Semiconductor
I²C devices through I²C (ch4)	[3.3 V] CN31: Touch screen connector
I²C devices through I²C (ch2)	[3.3 V] U44: ADV7511WBSWZ by Analog Devices U22: ADV7180WBCP32Z by Analog Devices U24: AK4642EN by AKM Semiconductor U50: R1EX24002ATAS0 by Renesas
I²C devices through I²C (ch1 port E)	[3.3 V] U37: DA9063 by Dialog Semiconductor

2.17. External Wait

2.17.1. Specifications

The R-CarM2 supports external wait requests from devices mapped to area 0 (CS0#), area 1 (CS1#), and expansion areas 0 to 5 (EX_CS0# to EX_CS5#). The R-CarM2 uses the LBSC to manage external waits.

The R-Car M2 Application Development Board does not incorporate a device to output WAIT or RDY requests. The only signal connected to the R-CarM2 is EXWAIT0#, which is output from the EXIO connector (CN23). The EXWAIT0# signal is pulled-up by a 10-kΩ resistor (R509) on the R-Car M2 Application Development Board, and a low level of this signal output to the R-CarM2 specifies a WAIT request.

Table 2.17.1 External Wait Control Interface Specifications

Signal	Devices that Output the WAIT or RDY Request
EX_WAIT0	(1) WAIT# request from the EXIO connector A (CN23)

2.17.2. Block Diagram

A block diagram of the external wait function is shown below.

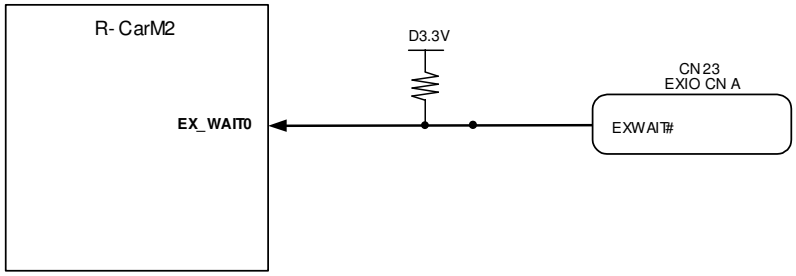


Figure 2.17.1 Block Diagram of External Wait Interface

2.18. External Interrupts

2.18.1. Specifications

The R-CarM2 has external interrupt input pins NMI, IRQ[9:0], INTC_IRQ[4:0]#, and INTC_EN[1:0]#.

The R-Car M2 Application Development Board uses IRQ0, IRQ1, and IRQ2 as external interrupt input pins. It also uses GP3_29 and GP6_29 as GPIO interrupts. These pins should be used as active-low signals in programs.

For the interrupt functions of the R-CarM2, see the R-Car Series, 2nd Generation User's Manual:Hardware.

The devices and connectors of the interrupt request sources on the R-Car M2 Application Development Board are shown below.

Table 2.18.1 External Interrupt Specifications

Interrupt Pin	Devices that Output Interrupt Request	Connectors
IRQ0	RMII PHY U21: KSZ8041RNLI by Micrel	
IRQ1	Touch Screen	CN31: GB10BXHAMLFSNP
IRQ2	PMIC U55: DA9063 by Dialog Semiconductor	
GP3_29	HDMI transmitter U44: ADV7511WBSWZ by Analog Devices	
GP6_29	Clock Synchronized Serial Device	CN6: 6-pin header

2.18.2. Block Diagram

A block diagram of external interrupts is shown below.

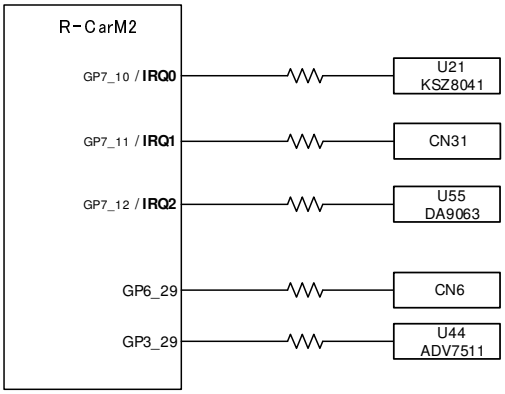


Figure 2.18.1 Block Diagram of External Interrupts

2.19. PWM

The R-CarM2 incorporates a seven-channel pulse width modulation timer (PWM). On the R-Car M2 Application Development Board, the use of other pin functions is given priority over the PWM functions in the case of pins that have multiplexed PWM functions. See the table below for details.

Table 2.19.1 Pin Functions Given Priority over PWM Functions

PWM	Pin Functions Given Priority over PWM Functions
PWM0	SD1_CD to SDHI1 interface
PWM0_B	GPIO (GP5_30)
PWM1	Mode pin 'MD8'
PWM1_B	SD1_WP to SDHI1 interface
PWM2	LBSC 'BS#'
PWM2_B	LBSC address 'A0'
PWM3	GPIO (GP1_24)
PWM4	GPIO (GP3_26)/DU1_DOTCLKOUT1
PWM4_B	Mode pin 'MD0'
PWM5	GPIO (GP7_21)
PWM5_B	GPIO (GP7_20)
PWM6	GPIO (GP7_22)

2.20. Clock

The R-Car M2 Application Development Board uses the crystal oscillators and resonators shown below.

2.20.1. Clocks Supplied to the R-CarM2

Table 2.20.1 List of Clocks and Crystals for R-CarM2

No.	Xn	Frequency	Pin Name on R-CarM2	Type	Remarks
1	X1	48.0000 MHz	USB_XTAL, USB_EXTAL	Resonator	-
2	X16	74.25 MHz	DU1_DOTCLKIN	Oscillator, socket-mounted	-
3	X3	148.500 MHz	DU0_DOTCLKIN	Oscillator	-
4	X4	14.7456 MHz	SCIF_CLK	Oscillator	-
6	X7	20.0000 MHz	EXTAL	Oscillator	(*2)

2.20.2. Clocks Supplied to Devices Other than R-CarM2

Table 2.20.2 List of Clocks and Crystals Other than for R-CarM2

No.	Xn	Frequency	Device	Device Pin Name	Type
1	X9	25.0000 MHz	IDT5V41066	X1, X2	Resonator
2	X8	25.0000 MHz	KSZ8041RNLI	XI, XO	Resonator
3	X13	12.0000 MHz	ADV7511WBSWZ	CEC_CLK	Oscillator
4	X11	28.63636 MHz	ADV7180WBCP32Z	XTAL	Oscillator
5	X14	11.2896 MHz	AK4642	MCKI	Oscillator
6	X18	32.768 kHz	DA9063	XTAL_IN, XTAL_OUT	Resonator

2.21. Power Supply

2.21.1. Specifications

The R-Car M2 Application Development Board operates on a single 12.0-VDC power supply.

The power supplies used for the R-Car M2 Application Development Board are generated by the switching regulators and low-dropout regulators.

Take care to ensure the following two points:

(1) Specified sequences should be used to turn on and off the power supply to the R-CarM2. Be sure to control the ACC switch (SW26) to obey the power sequence on the R-Car M2 Application Development Board.

See the table below for regulators used to generate power supplies on the R-Car M2 Application Development Board, their input voltage (Vin) and output voltage (Vout), and whether the ACC switch can be used to enable or disable output of power supplies.

Table 2.21.1 List of R-Car M2 Application Development Board Switching Controllers and Regulators

Vin	Vout	Switching Controller and Regulator	ACC Switch Control
Power Supply 12.0 VDC through CN25	D12.0V	-	Not supported
D12.0V	D5.0V / VSYS	IR 3838 (U576)	Supported
	D1.35V / B1.35V	Rich Technology RT7239 (U575)	Supported
D5.0V	VTT	Richtek USA RT9026 (U29)	Supported
	D1.8V	Dialog Semiconductor DA9063 (U55)	Supported
	D1.0V	Dialog Semiconductor DA9063 (U55)	Supported
	D3.3V	Dialog Semiconductor DA9063 (U55)	Supported
	D1.8V_PERI	Dialog Semiconductor DA9063 (U55)	Supported
	VCCQ1.8V	Dialog Semiconductor DA9063 (U55)	Supported
	VLDO3_SD0 (3.3 / 1.8 V)	Dialog Semiconductor DA9063 (U55)	Supported
	VLDO4_SD1 (3.3 / 1.8 V)	Dialog Semiconductor DA9063 (U55)	Supported
	VIO33 (3.3 V)	Dialog Semiconductor DA9063 (U55)	Supported
	VLDO7_1.8V	Dialog Semiconductor DA9063 (U55)	Supported
	VLDO8_SD2 (3.3 / 1.8 V)	Dialog Semiconductor DA9063 (U55)	Supported
	DVFS1.0V	Dialog Semiconductor DA9210 (U56)	Supported

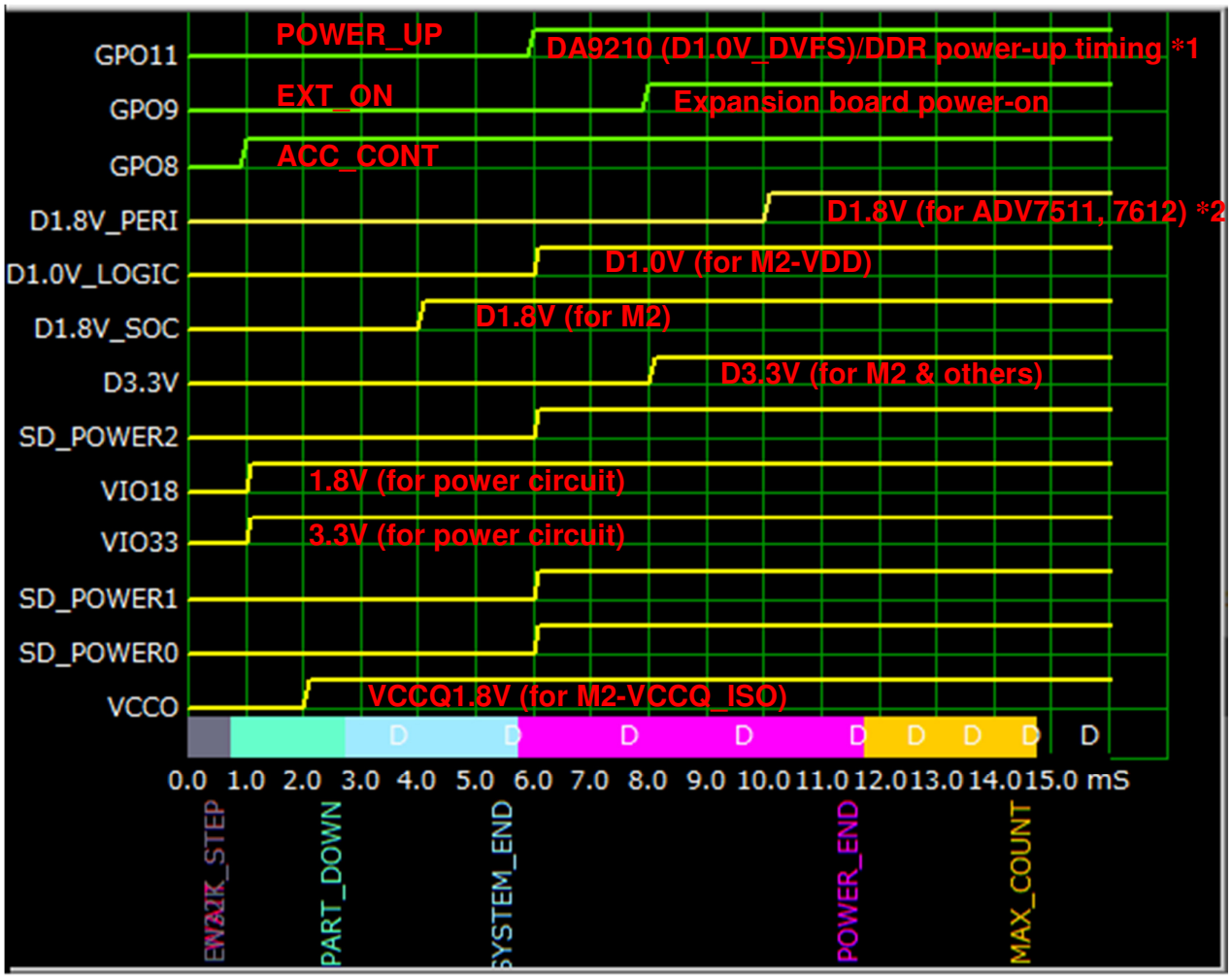
[Note]

As D12.0V is output to the following connectors, connecting or disconnecting an external board or a cable to these connectors must be performed while 12 V is not supplied to CN25 (while the 120-VAC switch is off).

- Power supply header (CN2)
- Power supply connector for serial-ATA interface (CN4)
- Connector for PCI Express (CN5)
- Back Light Header Connector (CN31)

2.21.2. Power-On Sequence

The diagram of the sequence for turning on the power (DA9063 OTP) to the R-Car M2 Application Development Board is shown below.



*1 The Co-PMIC (DA9210: D1.0V_DVFS) and DDR power (RT7239: D1.35V, B1.35V) are turned on with the power-up timing.
*2 In the power-off sequence, turn off the power supplies in reverse order of the power-on sequence.

Figure 2.21.1 Power-On Sequence

3. Outline Diagrams of R-Car M2 Application Development Board

3.1. External Dimensions and Hole Locations of R-Car M2 Application Development Board

The following shows the external dimensions and hole locations of the R-Car M2 Application Development Board. (Unit: mm)

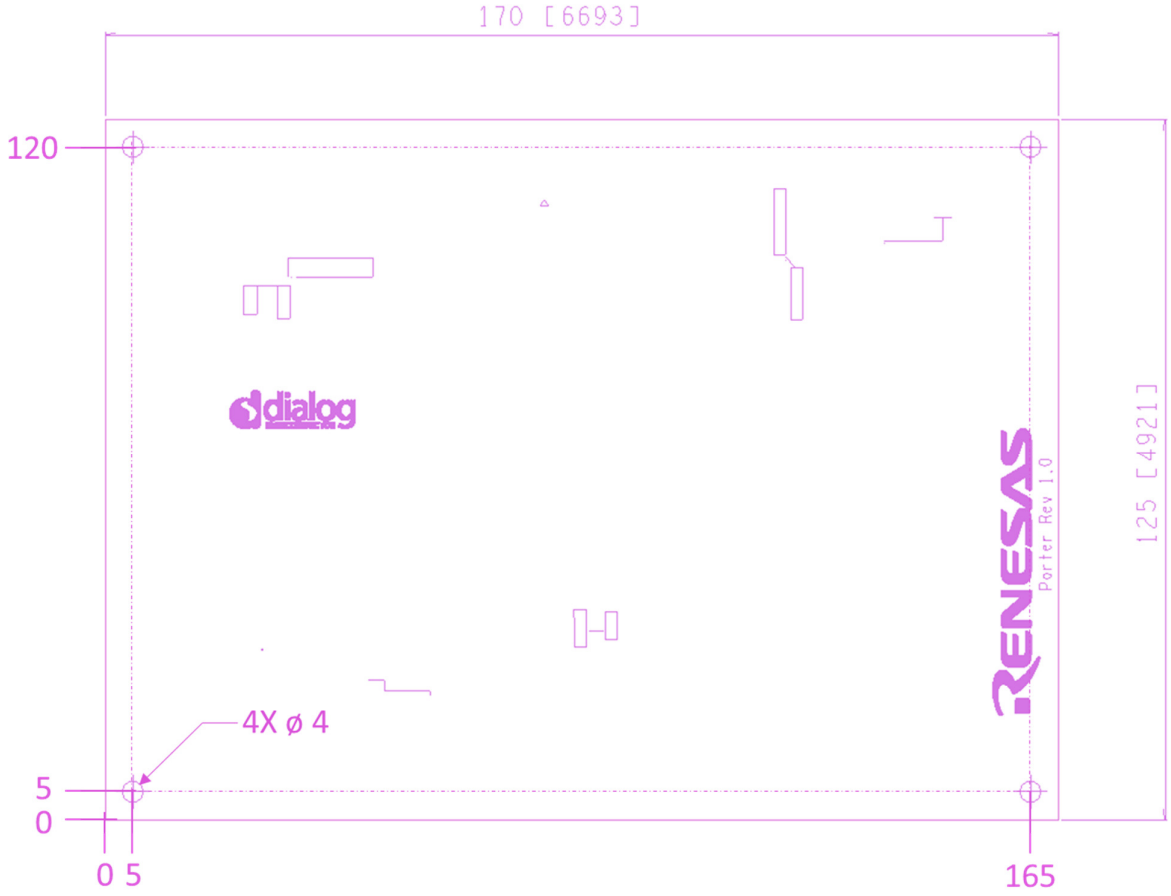


Figure 3.1.1 External Dimensions and Hole Locations of the R-Car M2 Application Development Board (Top View)

3.2. Connector Locations on R-Car M2 Application Development Board (Component Surface)

The following shows the connector locations on the component surface. (Unit: mm)

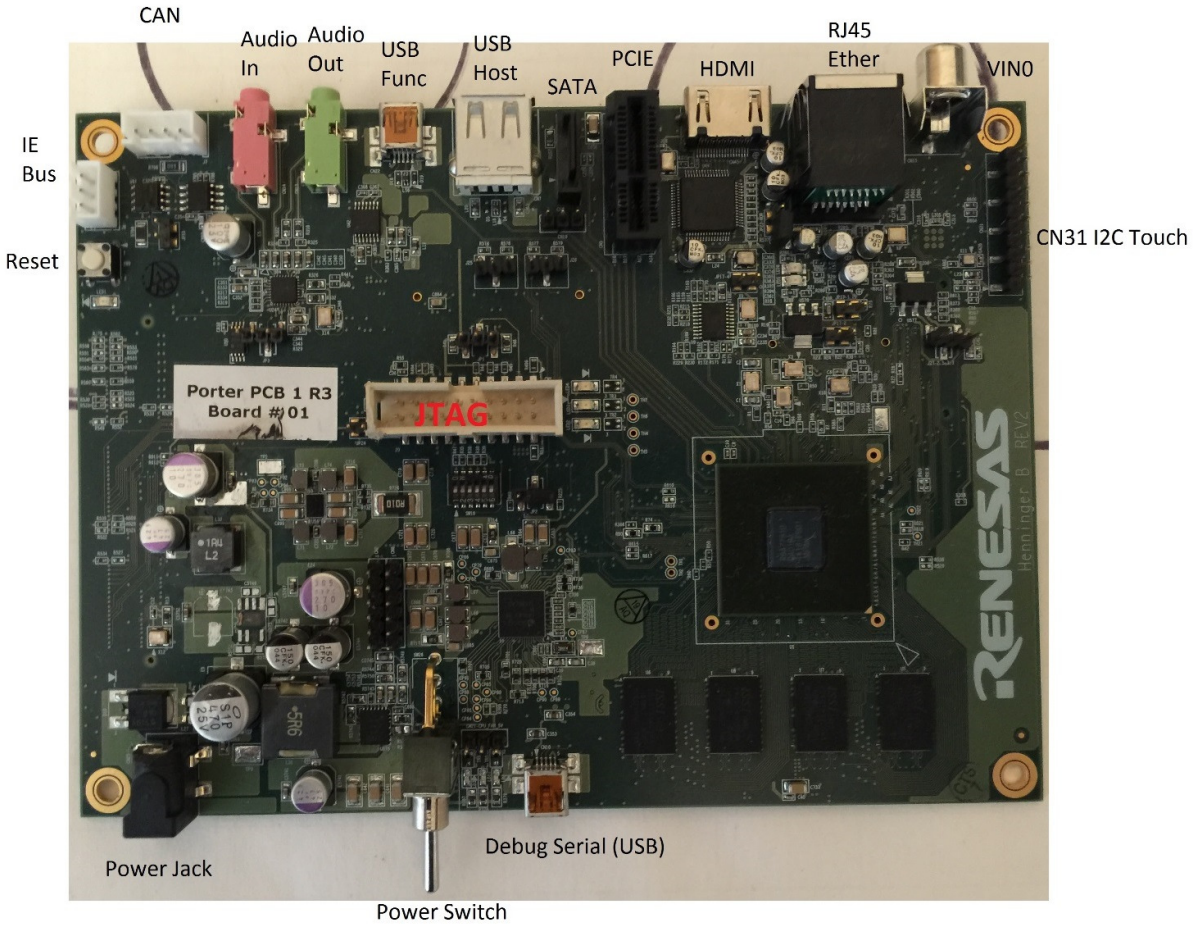


Figure 3.2.1 Connector Locations of the R-Car M2 Application Development Board (Component Surface) (Top View)